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INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Simon DELEONIBUS		
Sheet 1 of 1		FILING DATE September 6, 2006		

U.S. PATENT DOCUMENTS				
Examiner Initials	Cite No.	Document Number	Date	Name
/W.W.K./	1	2004/0014276	01/22/2004	MURTHY et al.
/W.W.K./	2	2001/0020725 A1	09/13/2001	OKUNO et al.
/W.W.K./	3	6,187,641 B1	02/13/2001	RODDER et al.

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
/W.W.K./	4	JP A 63-122177	05/26/1988	JAPAN	X	
/W.W.K./	5	JP A 63-013379	01/20/1988	JAPAN	X	
/W.W.K./	6	JP A 01-112772	05/01/1989	JAPAN	X	
/W.W.K./	7	JP A 61-276265	12/06/1986	JAPAN	X	

OTHER DOCUMENTS						
Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)				
/W.W.K./	8	Subramanian, V., et al. "A Novel Technique for 3-D Integration: Ge-seeded Laterally Crystallized TFTs." <i>1997 Symposium on VLSI Technology -- Digest of Technical Papers</i> , pp. 97 - 98, June 10, 1997.				
/W.W.K./	9	Lindert, N. et al. "Quasi-Planar FinFETs with Selectively Grown Germanium Raised Source/ Drain." <i>2001 International SOI Conference Proceedings</i> , pp. 111-112, October 1, 2001.				

EXAMINER	/W. Wendy Kuo/	DATE CONSIDERED 10/24/2007
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Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: September 6, 2006